In the Claims

Please cancel claims 1-29 and add new claims as indicated.

1-30. (cancelled)

31. (new) A method comprising:

receiving a series of signals;

indicating in non-volatile storage a monotonic count of said received signals by performing, in order,

changing a selected bit from a first state to a second state upon receipt of each signal in said series of signals, wherein the selected bit begins with a least significant bit and continues through increasingly more significant bits with each subsequent one of said received signals, until a predetermined number of the selected bits have been changed to the second state;

returning the selected bits to the first state;

changing the selected bit from the first state to the second state upon receipt of each further signal in said series of signals, wherein the selected bit begins with a second least significant bit and continues through increasingly more significant bits with each subsequent one of said received signals, until the predetermined number of bits have been changed to the second state.

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32. (new) The method of claim 31, further comprising:

returning the selected bits to the first state;

changing the selected bit from the first state to the second state upon receipt of each further signal in said series of signals, wherein the selected bit begins with a third least significant bit and continues through increasingly more significant bits with each subsequent one of said received signals, until the predetermined number of bits have been changed to the second state.

33. (new) The method of claim 31, wherein:

said indicating in non-volatile storage comprises indicating in a non-volatile memory.

34. (new) The method of claim 33, wherein:

said indicating in the non-volatile memory comprises indicating in a flash memory.

35. (new) The method of claim 31, wherein:

said indicating in the non-volatile storage comprises indicating in a non-volatile register.

36. (new) The method of claim 31, wherein:

said predetermined number is ten.

37. (new) The method of claim 31, wherein:

said returning to the first state comprises erasing:

38. (new) An apparatus comprising:

non-volatile storage;

a controller to perform in the non-volatile storage, in order,

changing a selected bit from a first state to a second state upon receipt of each signal in said series of received signals, wherein the selected bit begins with a least significant bit and continues through increasingly more significant bits with each subsequent one of said received signals, until a predetermined number of the selected bits have been changed to the second state;

returning the selected bits to the first state;

changing the selected bit from the first state to the second state upon receipt of each further signal in said series of received signals, wherein the selected bit begins with a second least significant bit and continues through increasingly more significant bits with each subsequent one of said received signals, until the predetermined number of bits have been changed to the second state.

39. (new) The apparatus of claim 38, wherein:

said non-volatile storage comprises a non-volatile memory.

40. (new) The apparatus of claim 39, wherein:

C.1 cont'd.

said non-volatile memory comprises a flash memory.

41. (new) The apparatus of claim 40, wherein:

said first state is an erased state.

42. (new) The apparatus of claim 38, wherein:

said predetermined number is ten.

43. (new) The apparatus of claim 38, wherein:

said non-volatile storage comprises a non-volatile register.

44. (new) A system comprising:

a processor;

a volatilve memory coupled to the processor;

non-volatile storage coupled to the processor to perform, in order,

changing a selected bit from a first state to a second state upon receipt of each signal in said series of received signals, wherein the selected bit begins with a least significant bit and continues through increasingly more significant bits with each subsequent one of said received signals, until a predetermined number of the selected bits have been changed to the second state;

returning the selected bits to the first state;

changing the selected bit from the first state to the second state upon receipt of each signal in said series of received signals, wherein the

C1 Cont'd.

selected bit begins with a second least significant bit and continues through increasingly more significant bits with each subsequent one of said received signals, until the predetermined number of bits have been changed to the second state.

45. (new) The system of claim 44, wherein:

said non-volatile storage comprises a non-volatile memory.

46. (new) The system of claim 45, wherein:

said non-volatile memory comprises a flash memory.

47. (new) The system of claim 44, wherein:

said non-volatile storage comprises a non-volatile register.